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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)			Filing Date 30 May 2001		(	Group	
U.S. PATENT DOCUMENTS							
Examiner Initial*	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE  IF APPROPRIATE	
LW_	5,847,588	12/8/98	Bruce C. McDermott	327	144	12/30/96	
FOREIGN PATENT DOCUMENTS							
Examiner Initial*	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES   NO	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
"A Semidigital Dual Delay-Locked Loop" by Stefano Sidiropoulos and Mark A. Horowitz. IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997.							
EXAMINER		3 2	DATE CONSIDERED	1/2/04			
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